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ON-LINE MONITORING GUIDE FOR TECHNICAL PERSONNEL(U)  
NAVAL OCEAN SYSTEMS CENTER SAN DIEGO CA A C MACMURRAY  
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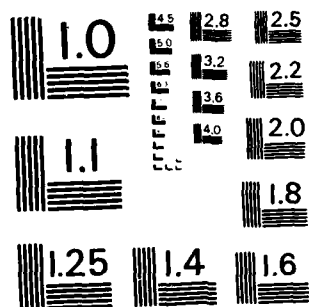
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## Technical Document 579

# ON-LINE MONITORING GUIDE FOR TECHNICAL PERSONNEL

AC MacMurray  
VD Leonard

7 March 1983

Final Report

Prepared for  
Naval Electronic Systems Command  
Test and Monitoring Systems Office  
Code 08T

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## SUMMARY

### OBJECTIVE

This Technical Document (TD) focus is on the on-line monitoring aspects of the overall topic of testability. The TD also summarizes the different performance monitoring (PM) design points. Off-line ATE points are already covered in other documents. This TD is aimed for the Engineering Designers rather than Project Managers although PM design should be part of a good RFP.

### APPROACH

*(performance monitoring)*  
The information in this ~~TD~~ *document* is broken down into monitoring hardware/software sections. It is applicable to various levels and types of systems. This TD begins with PM design selection and parameters, and covers various PM architectures and trade-offs. Next are components such as analog and electrical sensors, as well as computers and memory monitoring. The last section covers levels of interface along with coupling and shielding.

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## SECTION 1.0

### PERFORMANCE MONITORING

1.1 It is desirable that all subassemblies within a unit be monitored. Monitoring has two primary functions: (a) to monitor the status of the hardware and inform the operator of any malfunction, and (b) to aid in the location of failed components. The "general well-being" of a system or subsystem is monitored by means of end-to-end Built-in-Test (BIT). There may be similar tests for the subsystems and lower-level modules. For detection of failure, the subsystems could be sequenced automatically to provide the first step in fault localizations.

Continuous or on-line performance monitoring may be achieved by: (a) observing normal input and output signals and applying reasonable criteria based upon known system-transfer characteristics, and (b) time-sharing the input with test signals and examine the test response at the output. This is possible if the system can accommodate, on a time-shared basis, both the normal and test inputs.

It is important that primary functions be built to incorporate fail-safe generation. Also, the greatest priority should be placed on these systems to obtain the highest technical level.

1.2 BUILT-IN-TEST (BIT). BIT as considered here is an integral part of each unit of the electronic system, which may be removable, but which does not operate out of the system environment. The size and complexity of BIT will generally reflect the size and complexity of the system it is intended to cover. Reliability is generally accepted as being inversely proportional to system complexity.

1.3 PERFORMANCE MONITORING. A function which continuously or periodically scans a selected number of test points to determine if the system is operating within specified limits. It may include provisions for insertion of stimuli. Monitoring should be compatible with the electronic system circuitry to minimize possible loss of performance occasioned by its use. Performance monitoring and fault detection and isolation at a point should be available from a single sensor. Priority should be given to the monitoring of functions that are most important to the operational mission, that are basic to fault diagnosis, and are least reliable or least accessible.

1.4 MONITORING DESIGN. Monitoring functions are performed on-line, by exercising components and circuitry within the electronic systems, by use of software and hardware stimuli, or monitoring circuits. Monitoring shall require no external stimuli or measurement equipment, and required performance of an item should not be degraded.

**1.5 OPERATIONAL READINESS TESTS.** The operational readiness test should be designed to be functional in both the mission and maintenance environments. Performance below acceptable levels and, to the extent practicable, marginal or degraded functions shall result in an advisory or caution indicator being energized.

**1.6 AUTOMATIC INITIATION.** Continuous monitoring should be provided for those items which contain mission-critical failure modes. Monitoring of other items shall be on a selective basis, which considers both the false alarm rate and the consequences of BIT failure.

**1.7 FAULT DETECTION LEVEL.** Monitoring should provide a fault detection function as a GO/NO-GO visual indication, and shall detect failure and out-of-tolerance modes which represent at least 98 percent of all electronic system faults. The growth of the electronic system design, due to the incorporation of monitoring circuitry and devices, should not exceed 10 percent of the electronic system circuitry, parts, and devices. The apportioned failure rate of the monitoring circuitry and devices should not exceed 10 percent of the failure rate of the item or function being monitored.

**1.8 SELF-TEST.** Self-test provisions shall be incorporated into the electronic system as a means of testing the operational status of monitoring circuitry, as well as a means of ensuring unambiguous readouts.

**1.9 MONITOR CALIBRATION.** Monitor circuits which contain reference circuits or measurement devices shall allow isolation from the electronic system circuitry and permit injection of test signals. Adjustments must be readily accessible, and fault-indication devices must be visible while adjustments are being performed.

**1.10 INDICATORS.** For integrated or multi-mode systems, indicators for the various subsystems and equipment may be grouped together in an electronic system readiness advisory panel. The system-status indicators should provide GO/NO-GO indications of system readiness or functional status.

**1.11 MAINTENANCE PANEL.** If provided, a maintenance panel should be placed so it may be readily viewed and operated by maintenance personnel. It consists of a group of several visual-fault indicators that will indicate to maintenance personnel which UUTs have malfunctioned.

**1.12 PERFORMANCE MONITORING PARAMETERS.** Identify the parameters and quantities of interest that measure the overall performance of the system. These should be expressed in terms that are easily quantized for incorporation into each system.

**1.13 MONITORING THOROUGHNESS.** The thoroughness or level of detail to be provided by the self-test and performance monitoring capability is expressed by means of two parameters: timeliness and test coverage.

**1.13.1 Timeliness.** Timeliness is an expression of how often a test function is performed, and thereby expresses the delay between the occurrence of a problem and its discovery. Two categories of timeliness: (1) continuous (system-performance indications available instantaneously); (2) periodic (fixed interval between tests to ascertain system performance).

Continuous monitoring is limited to non-interfering on-line tests. Periodic monitoring primarily applies to interfering on-line tests, but also applies to non-interfering tests of complexity exceeding that which can be performed continuously. Manually initiated tests can be on-line or reconfigured but usually reflect test conditions that require operator intervention.

**1.13.2 Test Coverage** is defined as the required amount of monitoring to be performed for each timeliness value. The following descriptive parameters shall be utilized:

- o Percent of faults detected
- o Percent of false alarms
- o Minimum accuracy of monitored parameter(s)
- o Minimum parameter error detectable
- o Percent of false status indications

**1.14 OTHER POSSIBLE PERFORMANCE MEASURES.** If the monitoring circuit is passive, it cannot initiate a test for the presence of a given fault. Therefore, it seems reasonable to only attempt to measure how effectively it will monitor and validate module results given the data inputs which occur. The name, Monitoring Capability Index (MCI), indicates the potential to detect failures, given the input conditions necessary to produce detectable errors.

The level of monitoring capability depends upon three things: (1) The percent of the function monitored (function coverage); (2) The percent of the module fault conditions which can be detected given proper inputs (fault coverage) for the monitored portion of the circuit, and (3) The percent of time that the results are monitored (cycle coverage).

**1.15 CONSTRAINTS.** Constraints on the design of the performance monitoring capability of the system include the following:

**1.15.1 Duration** is the maximum duration of all reconfigured or interfering tests as well as a maximum time to recover from any test mode.

**1.15.2 Maximum Test Time** is the maximum time to perform all performance monitoring tests for a given operating cycle for the system over a given period.

**1.15.3 Cost** is a limit for the cost increase to the system for provision of system performance monitoring capability.

**1.16 SYSTEM VERSUS EQUIPMENT REQUIREMENTS.** Performance-monitoring goals for the system, and those defined for the equipment items that comprise the system will overlap.

Equipment testability in response to MIL-STD-454, Section 54 (Maintainability) and 32 (Test Provisions), will fulfill many of the requirements for performance monitoring of the system.

Interference and reconfigured testing, to ascertain correct performance of the equipment, should be minimized in those cases for which system on-line performance monitoring can provide the same information.

**1.17 MONITORING COMMONALITY.** Command hardware can often be put to a variety of uses. This is particularly true of computer-based systems. While programmed to fulfill different system requirements, many circuits can be exercised by means of standard test programs. The commonality of BIT hardware and software can be extended to all designs which use a standard computer or a fixed set of functional modules.

In the consideration of design, provision should be made for Automatic Test Equipment (ATE) accessibility, both to initiate the operation and to extract information. Monitor threshold must not be wider than the ATE threshold, or failures indicated by BIT will not be verified by the ATE. Usually, a combination of on-line monitoring and automatic test equipment (ATE) diagnostics will be employed in a given system.

**1.18 FAULT ISOLATION.** The level of BIT required to locate the malfunction is directly related to the Mean Time To Repair (MTTR) requirement for the system, which includes the total repair time, disassembly, replacement, reassembly, and checkout. The level must be sufficiently high to locate the malfunction to the smallest functional block feasible. This functional block may consist of one of several cards.

Standard techniques used to maintain reliability, in the face of increasing complexity, include the use of redundant and alternate circuits, and the incorporation of self-test capabilities. Thanks to the rapid advances made in integrated-circuit technology, weight, size, and power consumption, penalties have decreased.

Redundancy increases system complexity, weight, size, and power consumption. Trade-off studies of cost versus weight, and size versus reliability should be conducted on redundancy versus BIT for a given system.

Monitoring instrumentation will often provide for the detection of marginal situations, which alert an operator to an existing degraded situation, but will not require the system to be turned off. It could be ignored until a more suitable time for examining or correcting the marginal situation.

## SECTION 2.0

### MONITORING ARCHITECTURE, MODES, AND SIGNALS

**2.1 ARCHITECTURE.** The term "architecture" connotes the general philosophy of the design and engineering approach to performance monitoring for a given system or class of systems. Architecture capabilities should support data evaluation and control activities for performance monitoring.

**2.2 CENTRALIZATION VERSUS DISTRIBUTION.** Considerations to be traded-off include centralization of functions in the central system computer versus distribution among the equipments. The decentralized control must have the following characteristics:

- o Self-test capability
- o Isolation from other system data
- o Some type of synchronization with system functions

**2.3 ACTIVE VERSUS PASSIVE.** The interrogation of the modules by a microprocessor which then evaluates the response, is an example of active BIT. Passive BIT monitors system performance without the use of a test pattern generator. The attribute that distinguishes active from passive monitoring, in fact, is simply a test generator.

The passive BIT provides continuous, but incomplete evaluation, while the active BIT complements it with more complete, but not continuous evaluation. Active stimulus injection to the prime equipment can achieve higher fault coverage and known fault coverage. Passive monitoring of operational signals is less complex, inexpensive and has negligible interference to the equipment.

**2.4 TEST MODES.** The following test modes shall be addressed.

**2.4.1 ON-LINE VERSUS INTERLEAVED.** The passive BIT is on-line, and is in operation while the system is operating. The active BIT checks the modules when the system is not performing its mission. It is also possible that the whole system can be tested without interrupting operation. The latter is referred to as interleaving BIT. Interleaving can be a powerful means for maintaining confidence in a system, without disrupting its mission for running tests. Initiated test is used only when called upon manually, or by a computer response to an indicated failure. A popular approach is to use continuous on-line BIT to monitor the general well-being of the hardware, and to use initiated BIT to assist in locating the malfunction. Initiated BIT is also very useful in testing sections of the unit which, if tested continuously or periodically, could disrupt the normal flow of operation. Initiated BIT can be handled by a computer.

**2.4.2 Reconfigured.** Reconfigured tests shall be constrained by the following limits:

- o Maximum duration
- o Maximum-system restoration time
- o Coverage, detail and thoroughness
- o Personnel requirements
- o Use of resources and cost

**2.4.3 On-Line, Non-Interfering.** These shall be constrained by the following limits:

- o Coverage, detail and thoroughness
- o Maximum time between tests
- o Periodicity
- o Continuous coverage
- o Use of resources and cost

**2.4.4 On-Line, Interfering.** These tests shall be constrained by the following limits:

- o Procedure to prevent false actions
- o Extent and duration of interruption
- o Maximum time between tests
- o Coverage, detail and thoroughness
- o Use of resources and cost

**2.5 TEST MIX FOR PERFORMANCE MONITORING.** The architecture description shall provide guidance concerning the mix of tests to achieve complete performance-monitoring coverage without excessively impacting system availability.

**2.5.1 Operational Impacts.** Describe all features of the performance monitoring architecture that will impact the design of operational hardware or software of the system. Include all features presenting a potential hazard to safety or danger of false or irreversible action.

## **2.6 INDUCTIVE AND DEDUCTIVE MONITOR**

**2.6.1 Deductive Monitoring.** Deductive monitoring assumes that if a certain function is within its stated tolerance limits, then all the function variables must be within their tolerance limits.

**2.6.2 Inductive Monitoring.** Inductive monitoring concludes that if a specified set of measured functions are found to be within their stated tolerance limits, then a single unmeasured (and perhaps unmeasurable) function also must be within its stated tolerance limits. System performance is apparently judged by induction. If no module sends a failure signal, the system is considered operational.

**2.7 LEVEL-TESTED.** Monitoring can be designed to self-test the system level, subsystem-module level, printed-circuit-board level, or even part level. The level depends on the reason that monitoring is employed. Maintenance requirements and life-cycle-cost trade-offs must be considered in selecting the functional level tested.

**2.8 SOFTWARE VS HARDWARE.** The BIT portion of each module can be software or hardware BIT, though it is most likely hardware. Software BIT implies hardware in the form of a computer or microprocessor. Where existing system computer resources are not available, the microprocessor is an interesting candidate for BIT implementation.

**2.8.1 Software.** Software BIT offers many advantages. Software is particularly applicable to end-to-end testing. It can provide input stimuli to the system under test, and can monitor the output. It can determine a GO/NO-GO condition, and also provide diagnostics to isolate the fault to a functional area. Considerations to be kept in mind when designing a system utilizing software are:

- o It is essential to isolate the system data from the test data
- o When monitoring the output of a given functional area, it is essential to provide adequate tolerance
- o The input stimuli should be kept at a minimum level to minimize their effect upon performance
- o Existing data networks should be used wherever possible to reduce cost and provide testing of interface circuitry
- o The key to optimized fault isolation is judicious selection of monitoring points. Wherever possible, a common monitoring point should be utilized to test more than one functional area
- o The possible increase in computer size for the inclusion of BIT must be considered

**2.8.2 Hardware.** Hardware in the form of hard-wired-logic circuits, which are standard in the system, can also be used to realize BIT. Hardware has its greatest value in areas where software cannot be used efficiently. In these areas, the hardware can monitor the input and output, and ascertain whether the output result is correct.

**2.9 MONITOR DATA ACCESS.** Self-test and performance-monitoring information from the equipment is to be accessed by the evaluation and control function. The procedure must be consistent with the types of equipment to be used in the system.

**2.10 TEST SIGNAL/DATA INJECTION.** The following trade-off factors should be considered in the process of inserting test signals into the equipment, in supporting data evaluation, and control activities for performance-monitoring (PM) functions:

a. Use of unique equipment (hardware simulators) to provide these PM functions versus incorporation into equipment already a part of system

b. The role that BIT implementation in the equipment can play in supporting these PM functions, versus the additional circuitry to provide them. The potential for resultant circuitry duplication should be considered and avoided.

c. Nature of and location of data processing resources to support signal/data injection

**2.11 SIGNAL INJECTION POINT SELECTION.** Requirements for signals from performance monitoring to be injected to achieve calibration, or other detailed performance evaluations, should be identified along with injection points in the prime equipment. Maximum commonality with signal injection points and generators used for equipment BIT should be maintained.

**2.12 PERFORMANCE LIMITS.** Performance degradation by signal injection circuitry must be kept within specified limits. Examine all injected signals to insure sufficient decoupling when prime equipment is not in a test mode.

**2.13 CONTROL.** Signal injection points must operate under control of either monitoring, or external test equipment. This control should be exerted so that the most probable failure modes of the BIT will leave the injection signal decoupled.

## SECTION 3.0

### SENSOR APPLICATIONS

**3.1 ELECTRONIC SENSORS.** The overall sensing circuitry consists of the actual sensor, amplifying circuitry, and buffering circuitry to external test equipment. The sensing circuitry design should have minimal effect on the prime equipment, such that any failure mode of the sensing circuitry, will not degrade the performance of the system being monitored.

**3.2 SENSORS.** Passive sensors should be used in preference to active sensors wherever possible. Items to be considered in the selection of transducers are:

- a. Sensitivity, the ratio of output to unit-input for system resolution requirements
- b. Range, the maximum values to be measured
- c. Physical properties, must be compatible with the environment
- d. Loading effects and distortion must be minimal
- e. Frequency response

**3.3 PERFORMANCE LIMITS.** The sensing circuitry should not significantly degrade any of the signal parameters. Examine all test signals to insure that proper tolerance limits are set.

**3.4 CALIBRATION.** Sensors requiring calibration, initial or otherwise, should be avoided when possible. Reference or self-test circuits or critical elements that require calibration and a means of access for calibration, should be identified.

**3.5 SHIELDING.** All sensors shall be designed so interference caused by electromagnetic radiation is minimized.

**3.6 SENSOR LOCATION.** The sole purpose of integral sensors is to facilitate performance monitoring and fault isolation. The location of these sensors (test point selection) must be based on their ability to detect and to isolate faults in the prime equipment.

**3.6.1 Test Point Selection.** Test point selection should be biased so as to concentrate sensors in areas where failures are most likely to occur. The failure rates are used only in a relative sense, to bias test point selection to the areas in the system that are more likely to fail.

**3.6.2 Parameter.** If the parameter at a particular test point is extremely difficult to measure, that test point should be avoided even if two alternate test points are required. Most parameters can be sensed with cost-effective sensors.

**3.7 HULL MACHINERY SENSING.** The choice of a specific sensor/transducer depends on the physical variable being measured, the accuracy needed, the measurement reliability, the measurement-output requirements, and the transfer characteristics. The latter includes, for example, linearity, sensitivity and range. Size, cost and environment are also factors that must be considered for the selection of a sensor/transducer.

**3.8 SENSOR TYPE.** Many sensors produce a voltage signal related to the variable being measured. These types of sensors include:

- a. Thermocouplers
- b. pH electrodes
- c. Piezoelectric crystals
- d. Magnetic flowmeters

Still others produce a current output, such as the mechanical paramagnetic oxygen sensors, the solid state Integrated Circuits (IC's) and the polarographic CO<sub>2</sub> detector. Most sensors; however, do not produce an electrical output, and these outputs need to be converted into a useful electrical signal. Most commonly they are presented as displacement, resistance, inductance/reluctance or capacitance change.

**3.9 PRESSURE SENSING TECHNOLOGIES.** Pressure measuring systems probably vary over a greater range of complexity than any other type of measuring system. Commonly used electrical transduction elements include metallic and semiconductor strain gauges, potentiometers, piezoelectric elements, variable capacitance and variable inductance devices, and differential transformers. Transducers employing more esoteric principles, such as vibrating wire, magnetostriction, ionization photoelectricity, and electrokinetic potential are generally used in highly specialized applications, and in terms of life cycle cost may not be suitable for monitoring systems.

**3.10 TEMPERATURE-SENSING TECHNOLOGIES.** Temperature is among the most widely measured parameters. Liquid-in-glass thermometers, bimetallic elements, thermocouples, and resistance thermometers are widely used and are of great importance to the monitoring.

**3.11 NON-CONTACT SENSORS.** A non-contact sensor is a device that is installed on the equipment to be checked, without requiring any disassembly to increase significantly the diagnostic capability.

**3.12 PROCESS-CONDITION MONITORING.** The process-condition monitoring technique consists of analyzing the machinery functional parameters directly from sensor output and comparing with design-specification values.

**3.12 MACHINE-CONDITION MONITORING.** The machine-condition monitoring technique consists of monitoring signals emitted by the machine while operating. Such signals are often referred to as "secondary effects." The frequently encountered machine-condition-monitoring techniques are:

- a. Vibration analysis, ultrasonic, stress wave emission, contamination analysis, holography, thermal imaging

- b. Corona discharge, resistivity, capacity, and eddy current

## SECTION 4.0

### COMPUTER, MICROPROCESSOR, AND MEMORY MONITORING

**4.1 GENERAL PURPOSE COMPUTER AS A MONITORING COMPONENT.** The general purpose computer is an attractive candidate for monitor applications. With a library of test programs, a wide range of equipment could be serviced by a single computer. Where a computer is an integral part of the system, it can be time-shared to perform monitor functions.

With BIT concentrated in the computer, no testing can be performed unless the computer is operating properly. It is first necessary to verify the proper operation of computer main frame, peripherals, displays and controls before BIT can be started.

**4.2 INTERFACE.** The computer has a particular set of interface characteristics, such as the I/O bus and the direct-memory access (DMA port), which are generally not compatible with units not intended to be linked to the computer. Special interface hardware has to be provided.

**4.3 SYNCHRONOUS.** The computer and the unit under test are not necessarily synchronous with each other. The computer cannot be expected to monitor performance on a clock-by-clock basis. It may be necessary to develop summary, or status information for the computer and this requires additional hardware. The computer may be time-shared to perform a variety of tasks, and on-line monitoring would be occasional or sampled, rather than continuous.

**4.4 DIGITAL-TO-ANALOG CONVERTERS (DAC).** With the price and size of DACs continuing to decrease, one can liberally sprinkle them about, and route the single-line signals from each to a central monitoring area.

#### **4.5 MONITORING APPROACHES**

**4.5.1 Duplication.** One of the major approaches to monitoring at any level is to replicate the whole or a part of an operational circuit, and then compare the result of the two simultaneous computations.

**4.5.2 BIT Coding.** Another approach quite similar to replication is the use of coding. The motivation for use of BIT coding is a monitor which may be nearly as effective, but less costly than replicating and comparing.

**4.5.3 Error Detecting Codes.** Monitoring performance through the use of error detecting codes introduces a subtle distinction, not adequately characterized by the three ideas of input, function, and cycle coverage.

**4.5.4 Known Results.** The preceding two monitoring approaches are characterized by the fact that the desired answers for particular inputs are not known beforehand. It is possible to do monitoring of a simpler form when the desired answer can be established ahead of time. The motivation for pursuing this idea is based on the expectation that the cost of such a monitor would be significantly lower, and its applicability more universal than the replication or coding approaches discussed previously.

**4.6 MICROPROCESSORS AND MONITORING.** Large-scale integration has made the microprocessor readily available for printed-circuit board mounting. The microprocessor is designed to function as a microcomputer when power, a clock signal, and input/output peripherals are supplied. Thus, it becomes possible to construct, on a single printed-circuit board, a computer which can apply a programmed-test sequence while evaluating and presenting the test results. An additional desirable feature of the microprocessor, when used in a monitoring system, is its ability to be easily reprogrammed to alter the test sequence for improved efficiency or effectiveness. Microprocessors can be universally applied to provide a more uniform approach to monitoring. Along with firmware, which is specific to a given task, there could be a universal set of microroutines to exercise all components and to localize errors.

**4.7 EMULATION.** Based on the input, the sample monitor computes its version of the output, and compares that to the sample output to determine the status of the network.

A programmatic passive monitor could be utilized in a standard configuration to monitor a wide variety of processing elements or module functions. Although an increase in flexibility of application is gained from use of programmatic devices, there will often be an attendant reduction in speed. The programmatic monitor cannot, in general, perform computations in the same time frame as the operational modules in question.

**4.8 VOTING CIRCUITS.** To eliminate the resultant error caused by a failed logic element, voting circuits may be utilized. The voting circuit consists of several identical components which function continuously and in parallel, while a vote-taker circuit compares their outputs, and selects the circuit output to reflect the majority opinion. The effects of a fault in any one component are eliminated.

Voting circuits are not normally used in present designs, since they are not specified due to increased cost, space, and weight, but they certainly offer significant savings in terms of readiness, logistics and maintenance cost.

**4.9 MONITORING MEMORY MODULES.** The computer main memory can contain error-processing routines and periodic-monitoring, confidence tests. Control memory can handle initialization routines and microdiagnostics on failures. Secondary memory would perform assorted monitor diagnostic routines

**4.9.1 Memory Modules.** The memory-class modules are characterized by their ability to store data. The test approach for the memory modules includes a parity-generator checker as a standard approach to monitoring module-interface circuitry and interconnections. Additional BIT techniques which provide monitoring of data within the module are examined in the following subsections. This approach is based on Navy QED memory designs. Variance from QED parameters may require modifications to the monitor design. There are two basically different approaches to checking memory modules. One approach is off-line testing, and the other approach is on-line. The module monitoring is performed on real data in real time with no resulting limitation on system throughput or overall speed.

**4.10 MONITORING RANDOM ACCESS MEMORY (RAM).** Of the various methods of on-line testing, replication and coding are the most practical approaches for RAM testing.

**4.10.1 Duplication.** Replication of the memory circuits is a straightforward technique for providing error detection. This method of fault checking detects all errors in the memory, including multiple bit faults and addressing errors.

**4.10.2 Parity.** Coding techniques offer a significant reduction in hardware over duplication at the expense of a slight decrease in fault detection capability. Single-bit-per-word parity, the simplest coding technique is the most common memory-error-detection technique. This coding detects all errors in an odd number of bits which include all single-bit errors. The slight reduction in the fault detection capability of the parity approach is of little concern. Built-in-test using parity on the RAM modules can detect single-bit errors in over 99 percent of the module's gates.

The off-line mode of testing RAMs is a less practical BIT method.

**4.11 ROMS AND PROMS.** Read-only memories (ROMs) are another resource which can be applied effectively to monitoring, particularly in the control area. ROMs can store the responses for test or perhaps limited operating conditions and the ROM output signals can be matched to those of the circuit under surveillance. In addition to detecting errors, the ROM can also include information concerning the source of the error, and the identification of the defective module.

Field programmable read-only memories (PROMs) have grown in use to the point where they have overtaken ROMs in BIT systems. The major applications of PROMs are in minicomputers and microcomputers for resident members of a monitor system.

**4.12 MONITORING READ-ONLY MEMORIES.** ROMs function in the same manner as RAMs during ready cycles and can be tested using similar techniques. The coding and storage of the check bits for error correction is the same as the RAM, except that the code is programmed in other ROMs, and there is no code generation done on the module. The recommended BIT approach for the ROM module is word parity. The methodology for selecting the best BIT method is identical to the RAM module. Parity implementation provides a check on almost the entire memory module with a relatively small increase in hardware.

**4.13 FIRST IN-FIRST-OUT MEMORY (FIFO).** The FIFO memory is similar to the other memory modules when considering built-in-test. Provisions for parity are made by the manufacturers of the FIFO in that the circuits are designed to store non-bit data words. This fact makes parity checking the most economical of all BIT approaches, because a very small amount of additional hardware is needed.

## SECTION 5.0

### INTERFACE, COUPLING, SIGNALS AND PARAMETERS

**5.1 PERFORMANCE TEST AND MONITORING INTERFACES.** For the purpose of system self-test and performance monitoring, this TD shall emphasize standardization of interfaces across a class of similar systems or components. Designers shall be cognizant of the increasing utilization of standard-digital interfaces in the equipment. All test signals possible shall be converted to digital form, and formatted for transmission over a standard digital interface. The interfaces should reflect the complexity of the equipment, the complexity of the performance-monitoring functions, and location of data evaluation and control functions.

**5.2 LEVELS OF INTERFACE.** For the purpose of standardization, the interface can be viewed as consisting of three levels as shown in Figure 1. Level I consists of the test points and associated analog test signals. In Level II, the test signals are multiplexed and converted to digital format. In Level III, the test signals are available via a standard digital multiplex data-bus systems.

**5.2.1 Level I.** Level I is a concession to a need for faithful replication of some test signals ( for calibration), or interaction with very simple equipment and commonly used signals. Its use should be avoided for other than those cases. It may not be practicable in all cases to convert a test signal or its significant parameters to digital format. Due to very high relative cost to achieve faithfully reproduced signals by digital techniques, a Level I interface should be specified, and an analog interface be provided rather than digital.

**5.2.2 Level II.** Level II represents signal conversion to digital format and data multiplexing a number of signals within an equipment. This is provided that transmission distance is relatively short. All test signals shall have a unique address with respect to the prime equipment. In addition to the criteria applicable to Level I, the following information shall be required:

- a. Measurement signal of interest
- b. Analog-to-digital signal conversion factor
- c. Measurement signal address
- d. Signal identifying name
- e. Transmission mode.

**5.2.3 Level III.** Level III is the highest and most complex level of interface. Central-data-bus-control capability is associated with the performance monitoring capability. Level III may be specified for the following data transmission requirements:

- a. Raw (digitized) test data (and test point addresses)

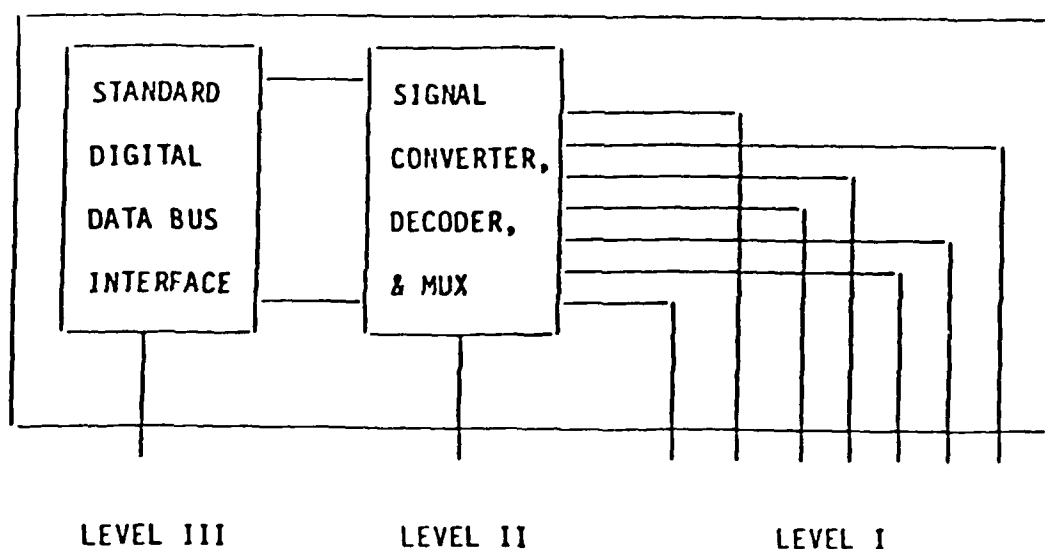


Figure 1. Levels of Interface

- b. Test results summary from local to central capabilities
- c. Command data
- d. Stimulus signals (and injection point addresses)
- e. Coded signal injection messages (to simulate local signal injection)

Level III interface exchanges processed self-test and performance monitoring information, data multiplexing, signal conversion, and interface functions by the data processing circuitry within the components.

**5.3 STANDARD INTERCONNECTION AND INTERFACE MONITORING.** A special circuit has been designed to provide the parity generation and checking necessary to implement the recommended technique. In addition, it was designed to provide parity generation and checking for the interconnecting data buses, as well as to detect wiring and connector faults. This special circuit is called the Standard Interface and Interconnection BIT (SIIB). The SIIB provides a module-level, on-line (concurrent) fault monitoring capability which can supply module pass/fail information to a system-fault monitor. Because of its multi-function design, it can be used in alternate ways to check different circuits, thus reducing the number of necessary standard BIT circuits. In addition, the SIIB provides an error detection and isolation capability for interconnecting circuitry, including logic card connectors, and backplane wiring. The BIT-functional approach embodied in the SIIB, is to check parity on incoming data and to check and to generate parity for outgoing data.

In the memory modules and certain IO modules, the parity-out data can be used to check the functional portion of the module. In this case, the SIIB circuit takes the place of a parity generator, and SIIB aids fault localization. In addition to checking the output buffers, the SIIB generates the parity bit to be transmitted on the bus along with the data bits. In order to verify the proper operation of the SIIB, a Force Parity Error (FPE) capability is included as a part of the SIIB circuit. The FPE line can be used to check not only the SIIB itself, but the associated wiring and subsystem-error-detection/localization-monitor hardware and software. The SIIB may be implemented with currently available off-the-shelf small- and medium-scale integrated circuits. An alternate approach would be to design a single custom Medium Scale Integrated (MSI) chip to realize the SIIB function. The single custom circuit is by far the most viable. Not only is the package count drastically reduced, but so is the failure rate and the power dissipation.

**5.4 INTERFACE.** System-monitoring interfaces pose problems of coupling and shielding. Interface should not interfere with mission operations. Interfacing is more difficult with active BIT than with passive. It is best to locate miniature Analog-Digital Converters (ADCs) at remote sensor sites, so data can be transmitted in digital format.

**5.5 COUPLING.** Different noise levels in a transmitter require that special coupling and isolation techniques be employed. Four methods of signal coupling follow:

**5.5.1 Line Drivers and Line Receivers.** The most common method of coupling monitor signals between units in which less than 10 to 15 volts of common-mode noise immunity is anticipated is the line-driver line-receiver combination.

**5.5.2 Transformer Coupling.** Currents which are monitored in transmitter high-voltage areas should be protected by a well-shielded current transformer.

**5.5.3 Coupling through Line Filters.** Another method of coupling, especially useful on slow signals, is one that uses a miniature EMI filter. Here, coupling from a noisy environment to a clean logic area can be made reliably in noisy areas since no active components are used.

**5.5.4 Optical Coupling.** The fourth method is optical coupling. It is useful where a difference in voltage, as high as many kilovolts, exists between the level of the sending unit and that of the receiving unit. Generally, the faster the devices, the smaller are the signals coming from the output of the coupler.

Fiber optics usually represent the safest method of coupling signals across a high-voltage interface. Optics are especially valuable for coupling BIT signals in transformerless power supply modulators, where all command signals arrive referenced with respect to ground. The most serious objection to using an optical transmission line has been the difficulty of repairing a broken line.

**5.6 SHIELDING.** Because of the possibility of a difference of DC or AC potentials existing between chassis grounds of the sending and receiving circuits, small signals in the millivolt range becomes rather questionable. Reliable circuits should normally be designed to operate with signals in the area from 5 to 12 volts. This produces a circuit with a reasonable size signal for use in transmitter noise environments. In transmitters especially, good shielding and proper grounding determine the BIT-fault-indicator accuracy to the greatest extent.

During high-voltage breakdown, extremely high magnetic fields occur, and magnetic shielding must be used to reduce magnetic field effects in areas where logic is located. Good shielding costs money, but good shielding results in superior indicator operation. It is best to shield against magnetic fields near their source.

Proper choice of the protective-logic family, with a good degree of noise immunity, is also beneficial to achieve the "failure-indicated" accuracy. There are several families of logic available.

**5.7 GROUNDING.** All output-measurement signals shall be measured relative to a common-equipment-circuit ground. Due consideration should be given to isolation, decoupling, and multiple/single-point-ground requirements

## **5.8 INTERFACE SIGNALS**

**5.8.1 Signal Characteristics.** Where possible, test signal characteristics (voltage level or frequency) shall be compatible with all equipments within the system which generate or process test signals.

**5.8.2 Analog Multiplexing.** Analog multiplexing under control of the equipment, should be utilized to minimize cable requirements where possible.

**5.8.3 Access of Non-Digital Signals.** Where required, an access should be provided for cabling to remote performance monitoring functions to enable them to obtain data from all analog test points. The cabling and associated connectors, and the signal amplifiers shall be compatible with the overall interface requirements for the system, without significantly degrading the test-signal quality. Signals shall be converted or shifted in level to match the signal constraints.

**5.9 PARAMETERS TO BE MONITORED.** The monitoring-function-tests parameters are key elements of the hardware. The number of tests required to detect all faults in large arrays using large numbers of integrated circuits, frequently cause test times to be impractical. Equipments and types of circuits are categorized as:

- a. Digital circuits, combinational and sequential
- b. Analog circuits
- c. Electronic equipments
- d. Electromechanical equipments
- e. Non-electronic systems.

Electronic circuit test parameters include:

- a. Voltage
- b. Current
- c. Equivalent current vectors
- d. Standard deviations of node voltages
- e. Time
- f. Power
- g. Frequency
- h. Nodal conductance, impedance, current, and voltage
- i. Reactance
- j. Word size
- k. Element current, voltage, and power losses
- l. Nodal voltage sensitivity
- m. Resistance
- n. Beta
- o. Mutual inductance

Digital parameters can be monitored as:

- a. Open - stuck at "1"
- b. Short - stuck at "0"
- c. Dynamic parameters

Analog-circuit test parameters consist of the same parameters as those of digital circuits; plus volume flow, pressure (hydraulic), torque, angular velocity, displacement (rotational), force, velocity (translational), temperature, stress, and strain

Analog parameters can be monitored as:

- a. Open
- b. Voltage
- c. Time
- d. Ratio
- e. Tolerance
- f. Frequency
- g. Power
- h. Set level

**5.10 MONITORING OF STRESS LEVELS.** The cost of a component and the ease with which it will be destroyed by the application of improper stress levels usually are the prime determinants as to whether a stress level shall be monitored. Limits on the percentage of voltage overstress allowed on a component are determined to some extent by expected transient levels, and through which an assembly must operate without serious degradation in performance.

The most critical of all measurements in a transmitter is a current monitoring of the final tube cathode current. This circuit is the one which demands the swiftest response in a transmitter and, along with other crowbar signals, requires faster response than a computer-controlled BIT can provide with its relatively slow response time. This is another place where the special BIT circuitry of the fault processor performs a vital function.

**5.11 INTERPRETATION.** Signal interpretation data will achieve commonality across equipment designs, and will simplify implementation of performance test and monitoring capability.

Descriptive information for test signals to be passed between equipment shall include:

- a. Signal label identifying the name of the signal
- b. Signal type (analog, digital, etc.)
- c. Signal description
- d. Signal multiplexing and data bus characteristics
- e. Multiplex address
- f. Other signal access requirements
- g. Signal interpretation (bit patterns, voltage levels, and other such physical or operational characteristics).

**5.12 CONNECTORS.** Performance monitoring connectors should be uniform over a given system, and be compatible with the interface standard selected. Connectors and cables should be compatible with the general cabling and connectors that are specified for the equipment in general.

**Appendix A**  
**ACRONYM GLOSSARY**

ATE	Automatic Test Equipment
ADC	Analog-Digital Converter
DAC	Digital-To-Analog Converter
DMA	Direct Memory Access
FIFO	First In-First Out
FPE	Force Parity Error
I/O	Input/Output
MCI	Monitoring Capability Index
MSI	Medium Scale Integration
MUX	Multiplexer
PM	Performance Monitoring
PROMS	Programmable Read-Only Memories
RAM	Random Access Memory
ROM	Read-Only Memory
SIIB	Standard Interface & Interconnection BIT

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